AI for Everyone, Everywhere

OPENEDGES

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The Future of AI Computing

OPENEDGES

Table of Contents

Openedges Technology at a Glance

99%

Sales Revenue CAGR(Last 5yrs)

* FY2019~2023

59

Number of Cumulative License Agreements

* As of June 30th

147

Global R&D Engineers

- 88% of total employees (168 members)
※ Largest among Korean IP Providers

AI for Everyone, Everywhere

OPENEDGES
Technology, Inc.

30+

Number of Clients

* Secured global top-tier customers such as Samsung Electronics, SK Hynix, and Micron

20+

IP products available for sale
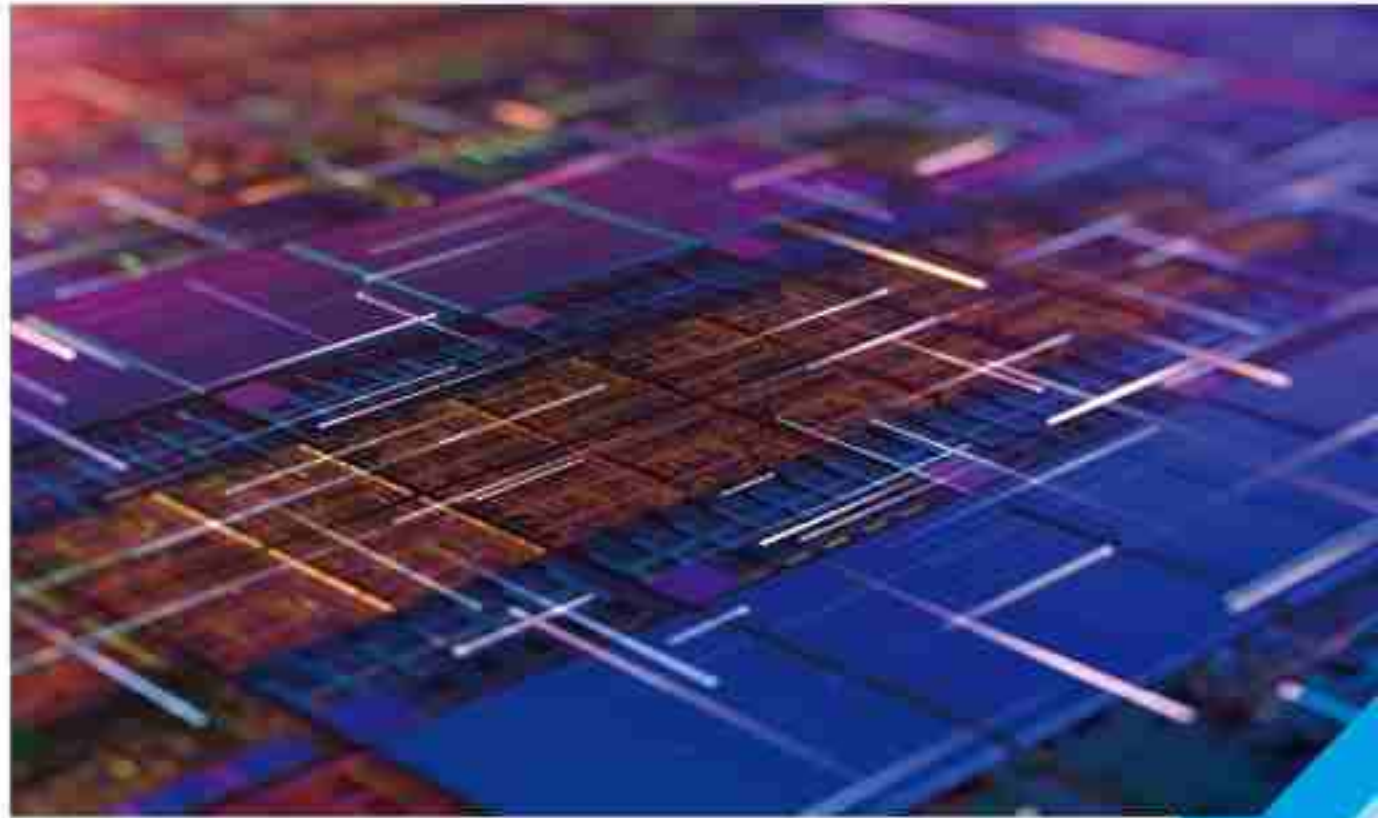
* Number of IP Products within 4 IP categories

4

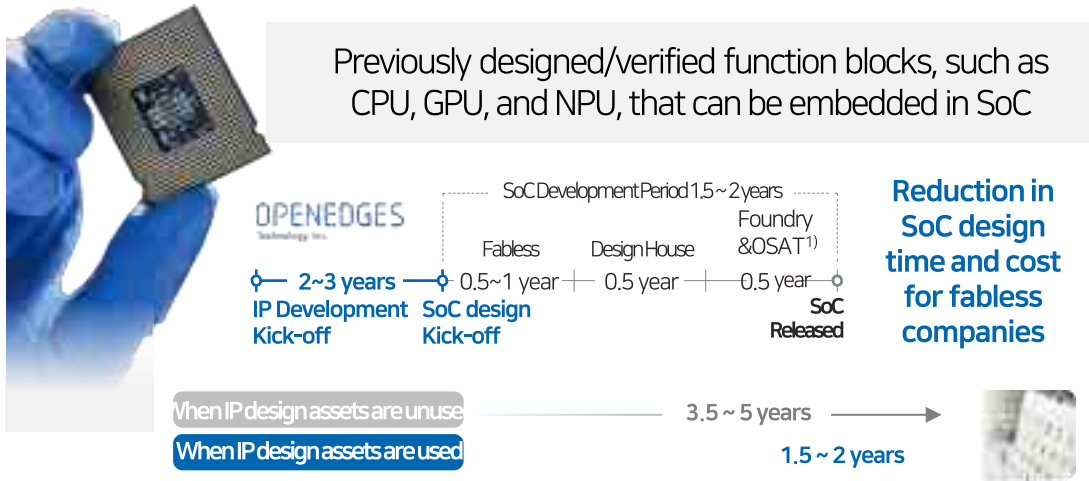Global R&D Centers

* Korea, US, Canada & Japan

Prologue

OPENEDGES Technology's Business Areas
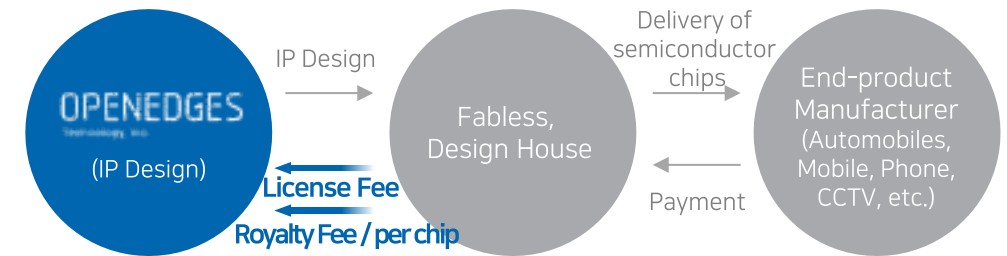
AI for Everyone, Everywhere

OPENEDGES Technology's Business Areas ①

Semiconductor IP is a ready-made solution requiring high-level technologies that enable faster development of SoC (System on Chip) such as AI semiconductors, reduce costs, and mitigate the risk of failure risks in development that can cost $100 million
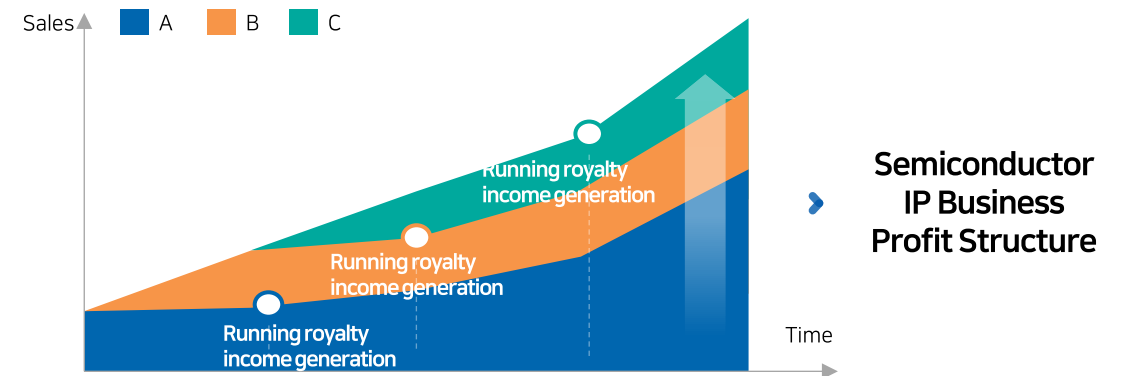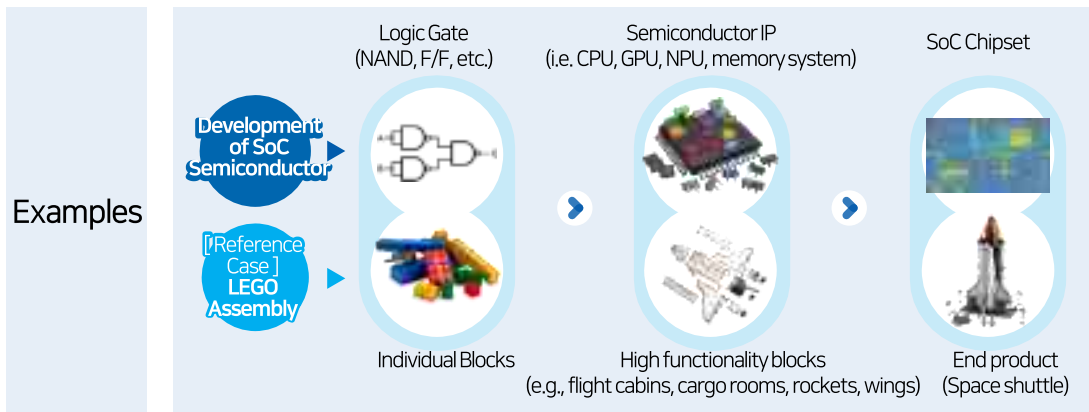
What is Semiconductor IP?

Previously designed/verified function blocks, such as CPU, GPU, and NPU, that can be embedded in SoC

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Technology Inc.

SoC Development Period 1.5 ~ 2 years

	Fabless	Design House	Foundry &OSAT[1]
2~3 years	0.5~1 year	0.5 year	0.5 year
IP Development Kick-off	SoC design Kick-off		SoC Released

Reduction in SoC design time and cost for fabless companies

When IP design assets are unuse — 3.5 ~ 5 years

When IP design assets are used — 1.5 ~ 2 years

Examples

Development of SoC Semiconductor

[Reference Case] LEGO Assembly

Logic Gate (NAND, F/F, etc.)	Semiconductor IP (i.e. CPU, GPU, NPU, memory system)	SoC Chipset
Individual Blocks	High functionality blocks (e.g., flight cabins, cargo rooms, rockets, wings)	End product (Space shuttle)

Business Model for IP companies

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Technology, Inc.
(IP Design)

IP Design →

Fabless, Design House

Delivery of semiconductor chips →

End-product Manufacturer (Automobiles, Mobile, Phone, CCTV, etc.)

← **License Fee**
← **Royalty Fee / per chip**

← Payment
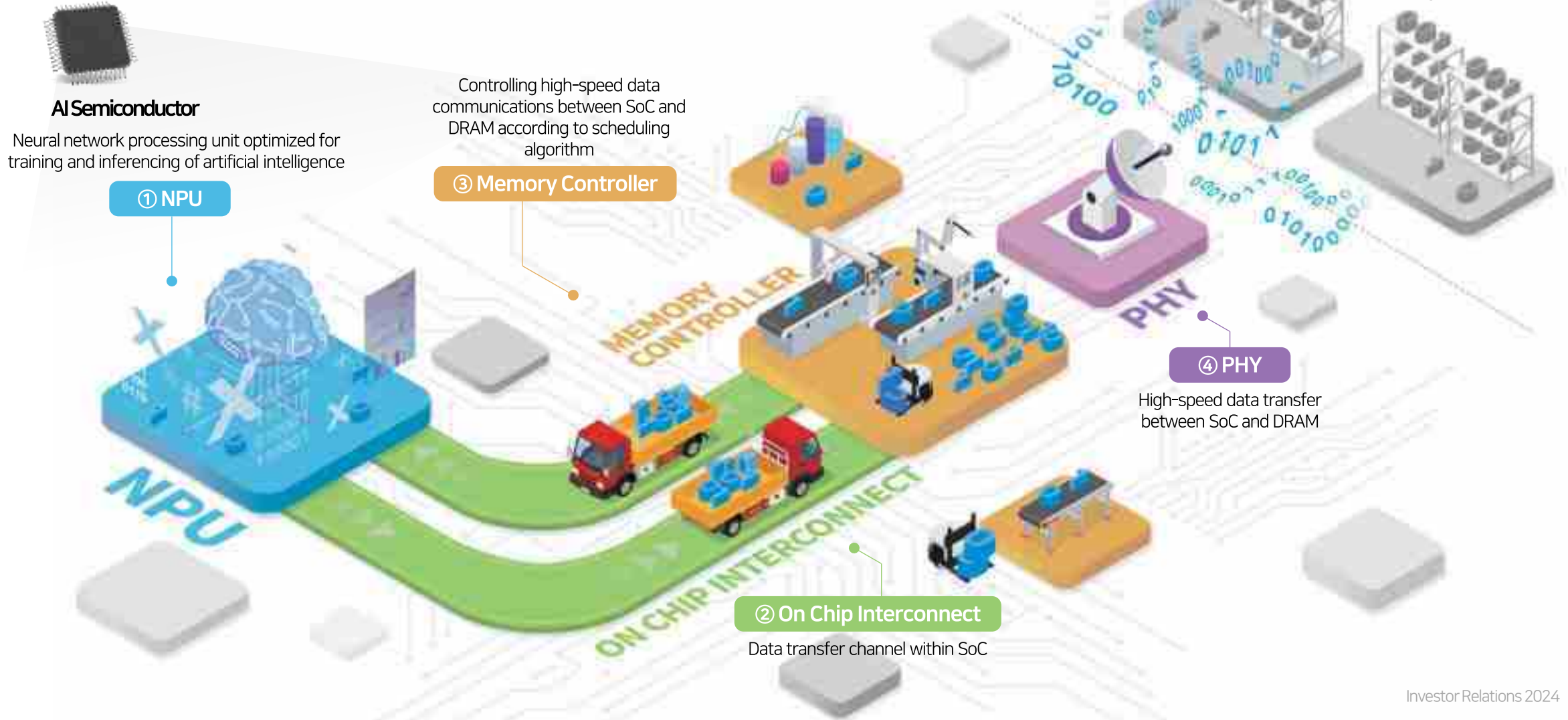
※ The semiconductor IP industry has been oligopolistic, dominated by a few market players due to high technical barriers to entry.

Sales | A | B | C

Running royalty income generation

Running royalty income generation

Running royalty income generation

Time

Semiconductor IP Business Profit Structure

※ Note 1) Outsourced Semiconductor Assembly and Test (Packaging and backend company)

OPENEDGES Technology's Business Areas ②

Design and provision of integrated IP solution that serves as a basis for AI semiconductor operation

DDR DRAM

AI Semiconductor

Neural network processing unit optimized for training and inferencing of artificial intelligence

① NPU

Controlling high-speed data communications between SoC and DRAM according to scheduling algorithm

③ Memory Controller

④ PHY

High-speed data transfer between SoC and DRAM

② On Chip Interconnect

Data transfer channel within SoC

01

Structural Development of System Semiconductor Market

01. Growth of AI Semiconductor & IP Market
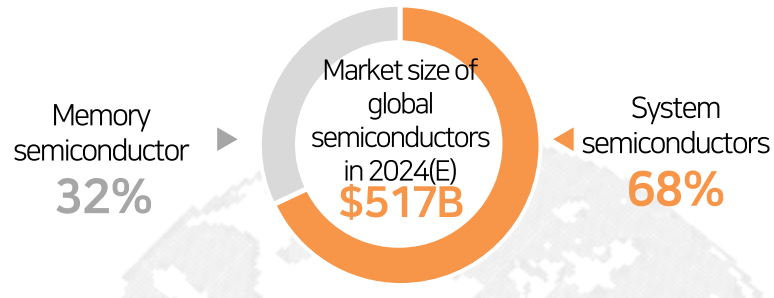02. Roles of Semiconductor IP Design Company

OPENEDGES
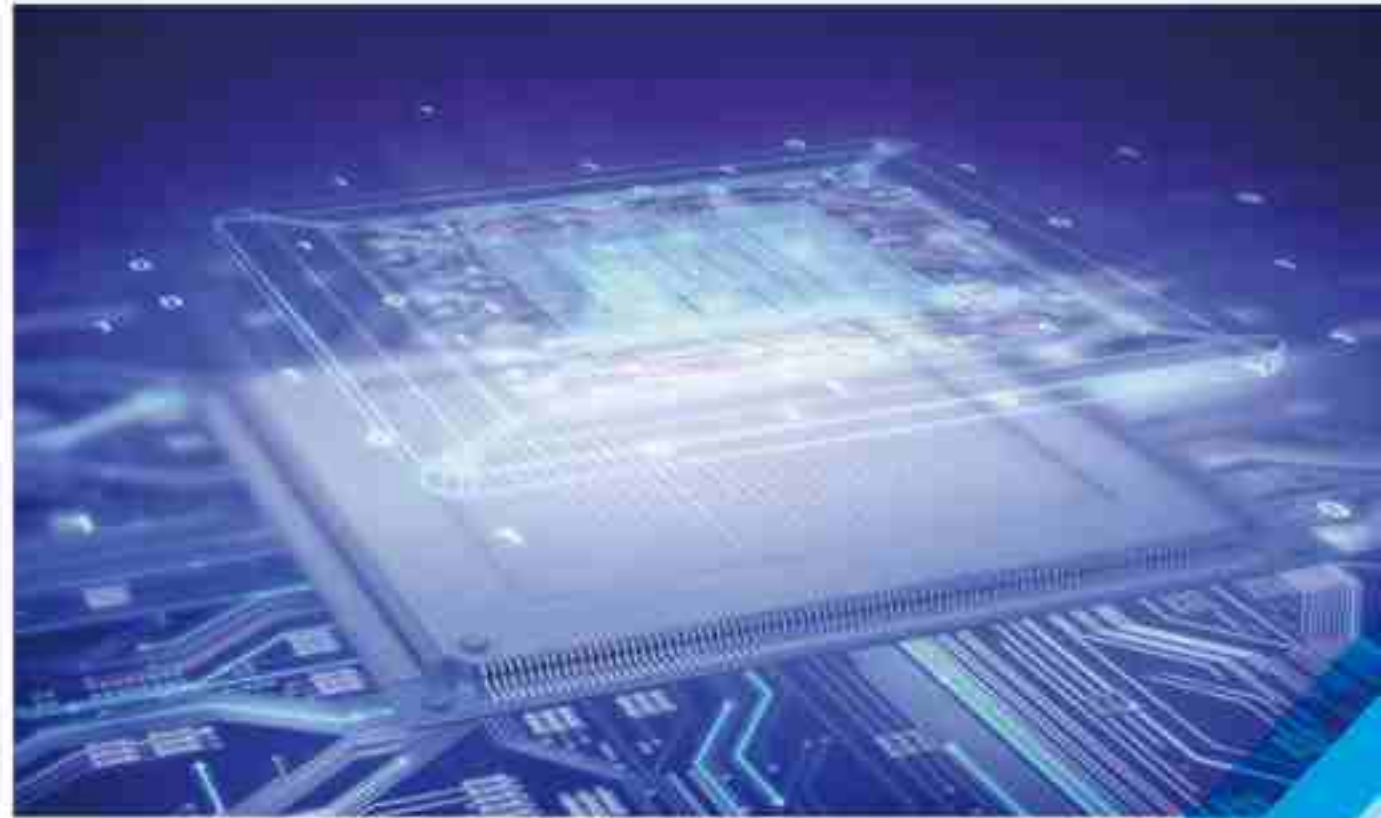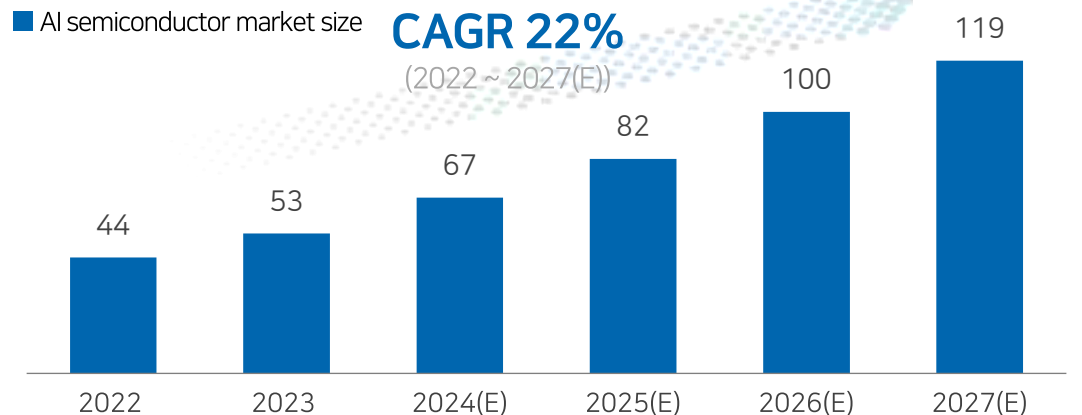
01 | Growth of Global System Semiconductor Market

Contrary to memory semiconductors, system semiconductors are continuing their steady growth

⫶ Prospects for Global Semiconductor Market 2024

Memory semiconductor **32%**

Market size of global semiconductors in 2024(E) **$517B**

System semiconductors **68%**

※ Source: WSTS, Nov 2023 (Excluding Optoelectronics, Discrete Semiconductors and sensors)

⫶ Global Semiconductor IP market forecast

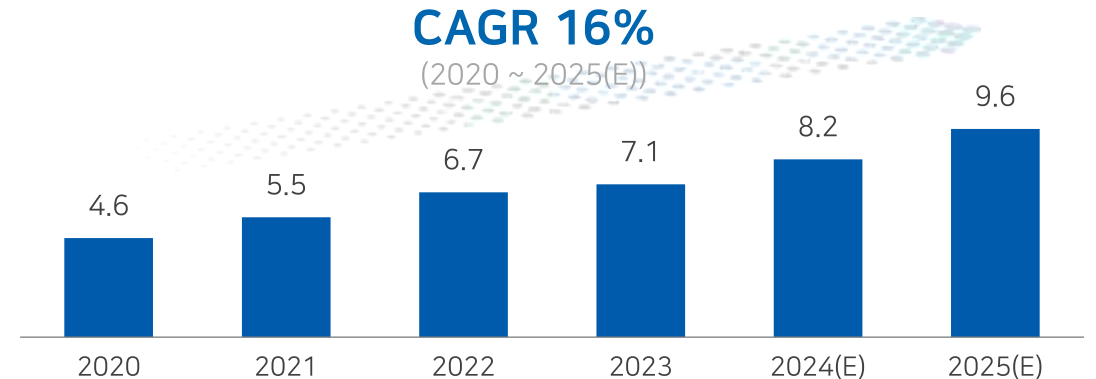| Company	2023 Sales ($ M)	CAGR ('19 ~ '23)
arm	2,938	10%
synopsys	1,542	17%
cadence	396	11%
OPENEDGES	15	99%
Others		14%
Total		16%

⫶ Prospects of Global AI Semiconductor Market

■ AI semiconductor market size

(Unit: $ B)

CAGR 22%
(2022 ~ 2027(E))

2022	2023	2024(E)	2025(E)	2026(E)	2027(E)
44	53	67	82	100	119

※ Source: AI Semiconductor (Gartner, Aug 2023), 당사추정

■ Semiconductor IP market size

(Unit: $ B)

CAGR 16%
(2020 ~ 2025(E))

2020	2021	2022	2023	2024(E)	2025(E)
4.6	5.5	6.7	7.1	8.2	9.6

※ Source: Design IP revenues (Ipnest, Apr 2024), Press Clipping

03 | Roles of Semiconductor IP Design Companies

Semiconductor IP companies aim to develop and supply function blocks as needed by Fabless and Design House in a proactive manner

System Semiconductor Ecosystem

Semicon-ductor IP Design Company → (Fabless) → Design House → Foundry → (O)SAT[1] →

	Semicon-ductor IP Design Company	(Fabless)	Design House	Foundry	(O)SAT[1]
Major Role	Design of major semiconductor function blocks	Semiconductor chip design (Frontend design)	Semiconductor chip design outsourced (Backend design)	Semiconductor chip manufacturing (Wafer processing)	Post-processing (packaging)
Number of players	Oligopolistic by ~50 companies	At least 3,000	N/A[2]	Top 10 M/S 97%	Top 25 M/S 50%
Size	$7.1B *The highest per-company market share	$170B	N/A	$104B	$50B
Major players	OPENEDGES, arm, synopsys, cadence	Qualcomm, NVIDIA, BROADCOM, MEDIATEK, AMD	GUC, GAONCHIPS, asicland, ADTechnology, SEMI FIVE	tsmc, SAMSUNG, PSMC, UMC	ASE GROUP, Amkor technology, JCET, SPIL

Reasons for IP oligopoly

Higher demand for proven IPs

VERIFIED

IP companies with proven IPs are in high demand due to the rising entry barriers

Requires highly proficient technical personnel

Requires R&D investments for at least 3 years

※ Note 1) (Outsourced) Semiconductor Assembly and Test: Semiconductor package assembly and test company that is responsible for performing post-processing after wafer process
Note 2) Design House market does not have a reliable market size data as it is in its initial formation stage.

02

OPENEDGES Technology, as Korea's most renowned AI semiconductor IP design company
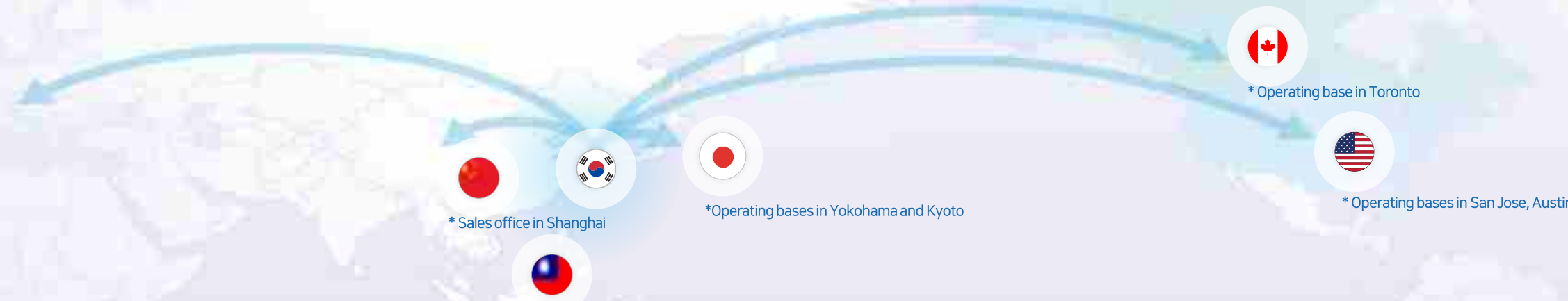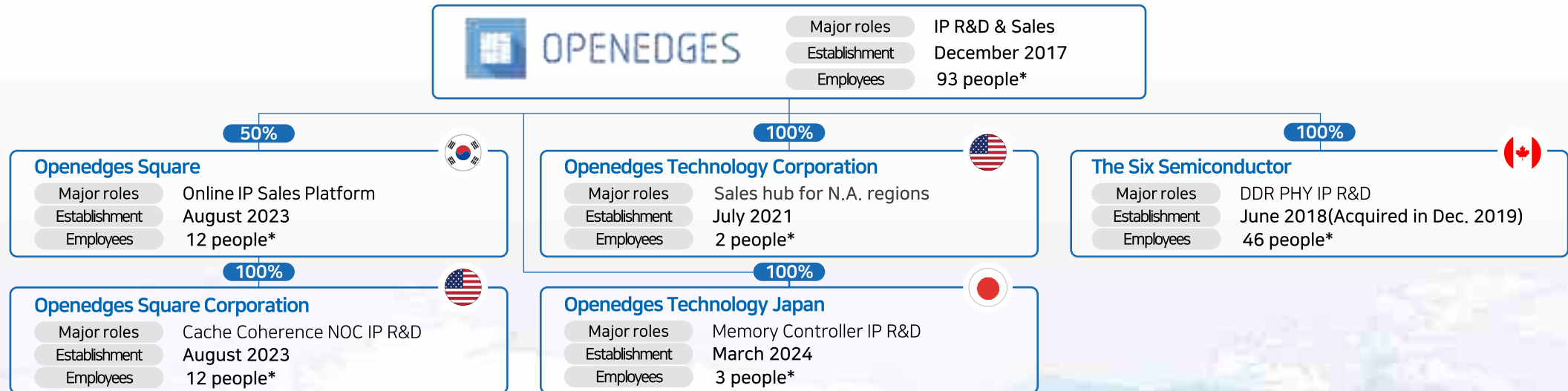
01 | The Overview of OPENEDGES' Core Competitiveness

OPENEDGES holds the key success factors
to become a global leader in the AI semiconductor IP market

01
A Global team of Professionals
★★★

02
Industry's highest technological competitiveness
★★★

OPENEDGES

03
Verified global track records
★★★

04
Strategic partnership with global enterprises
★★★
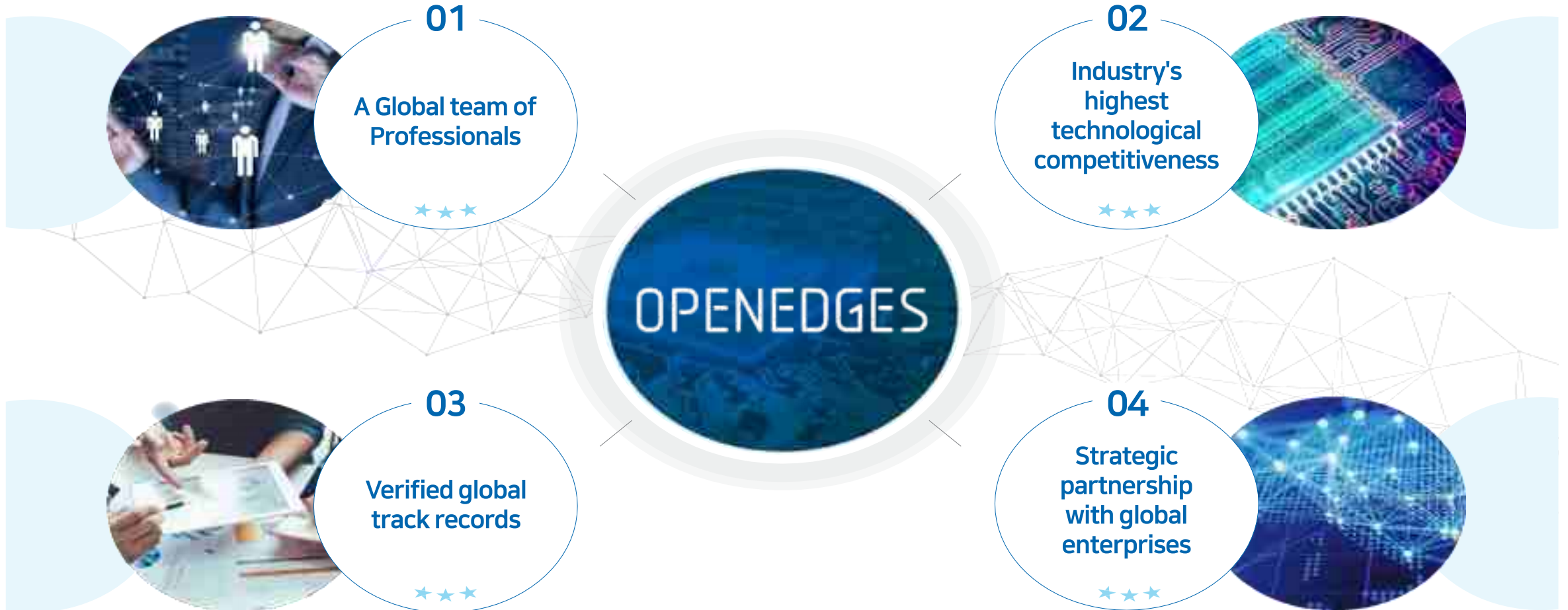
02 | A Global Team of Professionals – Global Presence

Expansion of global bases in addition to offices in the U.S., Canada and Japan

OPENEDGES

Major roles	IP R&D & Sales
Establishment	December 2017
Employees	93 people*

50%

Openedges Square

Major roles	Online IP Sales Platform
Establishment	August 2023
Employees	12 people*

100%

Openedges Technology Corporation

Major roles	Sales hub for N.A. regions
Establishment	July 2021
Employees	2 people*

100%

The Six Semiconductor

Major roles	DDR PHY IP R&D
Establishment	June 2018(Acquired in Dec. 2019)
Employees	46 people*

100%

Openedges Square Corporation

Major roles	Cache Coherence NOC IP R&D
Establishment	August 2023
Employees	12 people*

100%

Openedges Technology Japan

Major roles	Memory Controller IP R&D
Establishment	March 2024
Employees	3 people*

* Operating base in Toronto

* Sales office in Shanghai

*Operating bases in Yokohama and Kyoto

* Operating bases in San Jose, Austin

* Sales office in Taipei

* As of June 30th, 2024

02 | A Global Team of Professionals

Leadership of industry-leading experts with over 20 years of experience from Samsung Electronics/SK Hynix, and more.
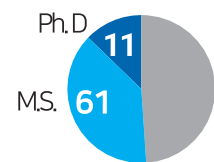
R&D personnel
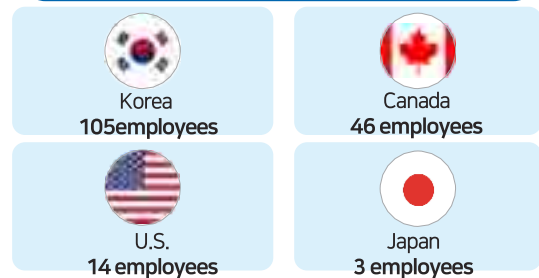
Among the total personnel (168 team members)

147 R&D personnel

88%

Percentage of Ph.D. and M.S. degree holders (72 members) among the R&D personnel

49%

Ph.D **11**

M.S. **61**

Status of Each Country

Korea
105 employees
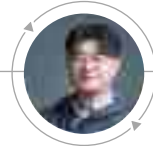
Canada
46 employees

U.S.
14 employees

Japan
3 employees

* As of June 30th, 2024

Sean Lee
Representative Director / CEO

SAMSUNG

Ph.D. Candidate in Electrical and Computer Engineering, Seoul National University
'17-Present: Representative Director, OPENEDGES Technology, Inc.
'08~'15: Principal Researcher, Samsung Electronics (Exynos Development)
'07~'08: Samsung Advanced Institute of Technology

Jake Choi
NPU Team Head

SK hynix | SAMSUNG

Ph.D. in Electrical and Computer Engineering, Purdue University
'18 ~ Present: NPU Team Head, OPENEDGES Technology, Inc.
'15~'18: Principal Researcher, SK Hynix
'09 ~ '14: Architecture Lab Part Head, Samsung Electronics

Richard Fung
TSS / CEO

AMD | PERASO

M.S. in Electrical and Electronic Engineering, Univ. of Toronto
'18 ~ Present: CEO, The Six Semiconductor
'12 ~'18: Silicon Director, etc., Peraso Technologies
'00 ~'11: PHY Analog Design Manager, AMD

Roger Jennings
OSC / VP of Engineering

ARTERIS | AMD | intel

M.S. in Electrical and Electronic Engineering, Univ. of Memphis
'22 ~ Present: VP of Engineering, OPENEDGES SQUARE
'20 ~ '22: Arteris IP Senior Director of Engineering
'00 ~ '21: Intel, Juniper Networks, AMD etc.

Cody Hwang
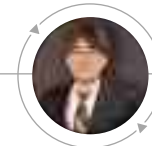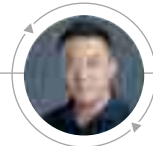R&D Center Head / CTO / Co-founder

대우전자 | Chips&Media

M.S. in Electrical Engineering, Seoul National University
• 2017- Present: CTO, OPENEDGES Technology, Inc.
• 2010-2015: CTO, CodeHolics
• 2000-2010: Daewoo Electronics, Chips & Media

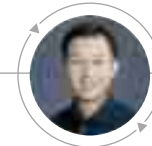**Takashi Yamada**
OTJ/Reginal VP

socionext | Panasonic

B.A in Electrical Engineering, University of Tokyo Denki
'24~ Present Openedges Technology Japan Regional VP
'15~'24 SOCIONEXT Inc., Principal Engineer
'88~'15 PANASONIC Corporation

Ricky Lau
TSS / CTO

AMD | SYNOPSYS

M.S. in Electrical and Electronic Engineering, Univ. of Toronto
'18-Present: CTO, The Six Semiconductor
'14 ~ '18: PHY Digital Design Engineer, Synopsys
'03 ~ '14: PHY Analog Design Engineer, etc., AMD

Niranjan Cooray
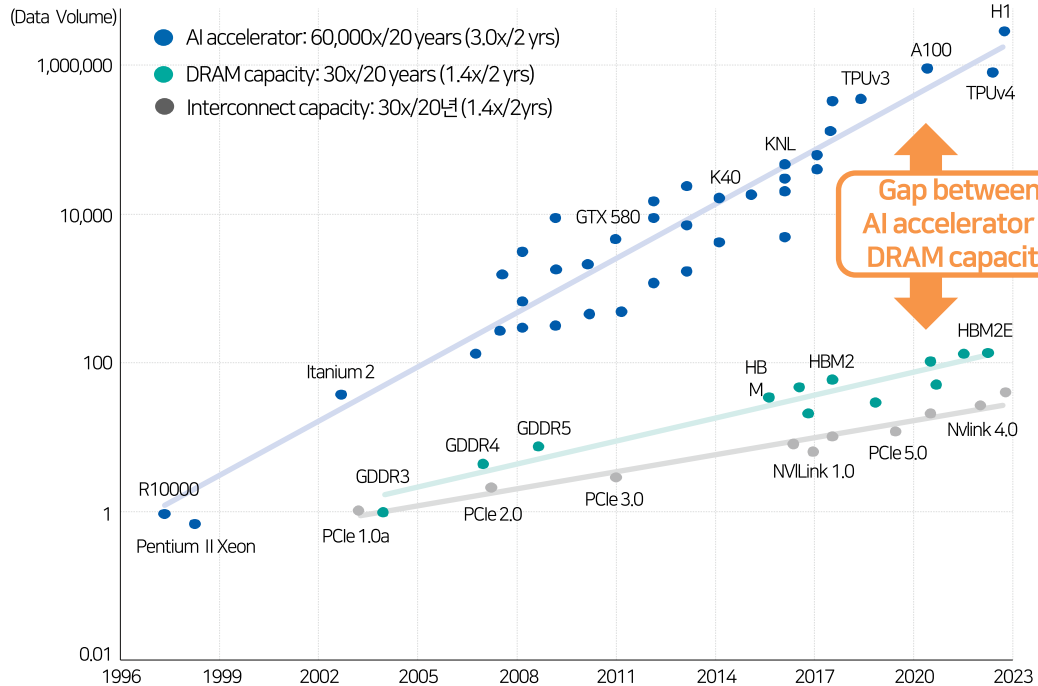OSC/Chief Architect

intel

M. S. in Electrical and Computer Engineering, Northeastern University
'24 ~ Present: OPENEDGES SQUARE, Chief Architect
'95 ~ '24: Intel, Principal Engineer

03 | Industry's Highest Technological Competitiveness ①

AI semiconductors are characterized as 'Data Intensive Computing'
→ Most optimize NPU and memory systems in edge AI with limited resources
OPENEDGES is the only global leading AI semiconductor IP platform provider

The gap between the required data processing volume and the capacity provided by DRAMs has increased due to the development of AI accelerator technologies

(Data Volume)

- AI accelerator: 60,000x/20 years (3.0x/2 yrs)
- DRAM capacity: 30x/20 years (1.4x/2 yrs)
- Interconnect capacity: 30x/20년 (1.4x/2yrs)

Gap between AI accelerator & DRAM capacity

※ Source: AI And Memory Wall By Riselab

AI Platform IP for Edge Computing

OPENEDGES is globally the only company that is capable of supplying NPU IP (the core of AI semiconductors) and memory system IP (functions as the 'Back Bone' for all semiconductors) at the same time.

NPU

Bare spot of AI semiconductor IP market filled by OPENEDGES

On-chip Interconnect

Memory Interface (Memory Controller + PHY)
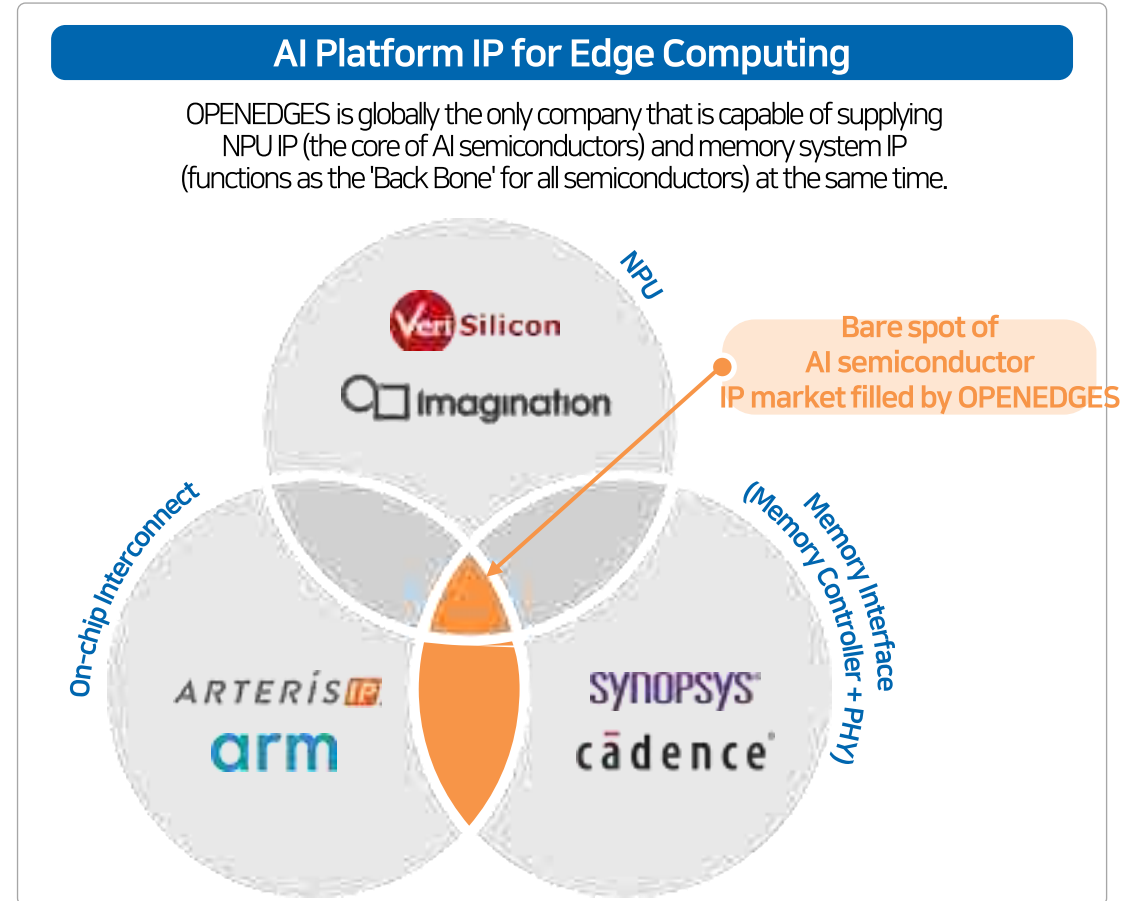
03 | Industry's Highest Technological Competitiveness ②

Leading the market through the development of cutting-edge technology

Division	IP	Description	Development Status	Remark
AI Platform IP Solution for Edge Computing	**ENLIGHT™ (Neural Processing Unit)**	ENLIGHT™-Light (0.25 ~ 2 TOPS)	Now	Lightweight IoT applications (Keyword recognition, security camera application)
		ENLIGHT™-Classic (2 ~ 16 TOPS)	Now	Intermediate IoT applications (ADAS)
		ENLIGHT™-Pro (16 ~ 250 TOPS)	**Now (Released in Apr. '24)**	**Automotive high-performance applications (Level 3 or higher self-driving vehicle application)**
		ENLIGHT™-Hyper (250 ~ 1000 TOPS)	In the future	Automotive high-performance applications (Level 4 or higher self-driving vehicle application)
Total Memory System Solution IP (ORBIT™)	**OMC™ (DDR Memory Controller)**	DDR4/3, LPDDR4X/4/3	Now	
		LPDDR5X/5/4X/4	Now	Current Mainstream Technology
		HBM3	Now	Server and ultra-high-performance products
		DDR5	Now	Current Mainstream Technology
		GDDR6	Now	High-performance AI product
		GDDR7	In the future	Next-generation High-performance AI product
		LPDDR6	**In the process**	**Next-generation Mainstream Technology**
	OPHY™ (DDR PHY)	LPDDR4X/4	Now	TSMC 22nm Nodes
		LPDDR5X/5/4X/4	Now	TSMC 16nm Nodes
		LPDDR5X/5/4X/4	Now	TSMC 12nm Nodes
		GDDR6	Now	TSMC 12nm Nodes
		LPDDR5X/5/4X/4	Now	TSMC 6/7nm Nodes
		HBM3	Now	TSMC 6/7nm Nodes
		DDR5	**Near future(~'25)**	**TSMC 5nm Nodes**
		LPDDR6	In the future	TSMC 4nm(or less) Nodes
		LPDDR3, DDR4/3	Now	Samsung 28nm Nodes
		LPDDR4X/4, LPDDR5/4X/4	Now	Samsung 14nm Nodes
		LPDDR5/4X/4	Now	Samsung 8nm Nodes
		LPDDR5X/5/4X/4	Now	Samsung 5nm Nodes
		LPDDR6	**Near future(~'25)**	**Samsung 4nm Nodes**
		GDDR7	In the future	-
	OIC™ (On-Chip-Interconnect)	OIC™	Now	Non- Cache-Coherent NoC
		OIC™-AI	In the process	Cache-Coherent NoC

03 | Industry's Highest Technological Competitiveness ③

Concentrate on areas that major global competitors cannot cover & expand M/S

DDR PHY IP Competition status   ☐ IP to be developed, ⭐: Sole Provider

Openedges | Synopsys | Cadence
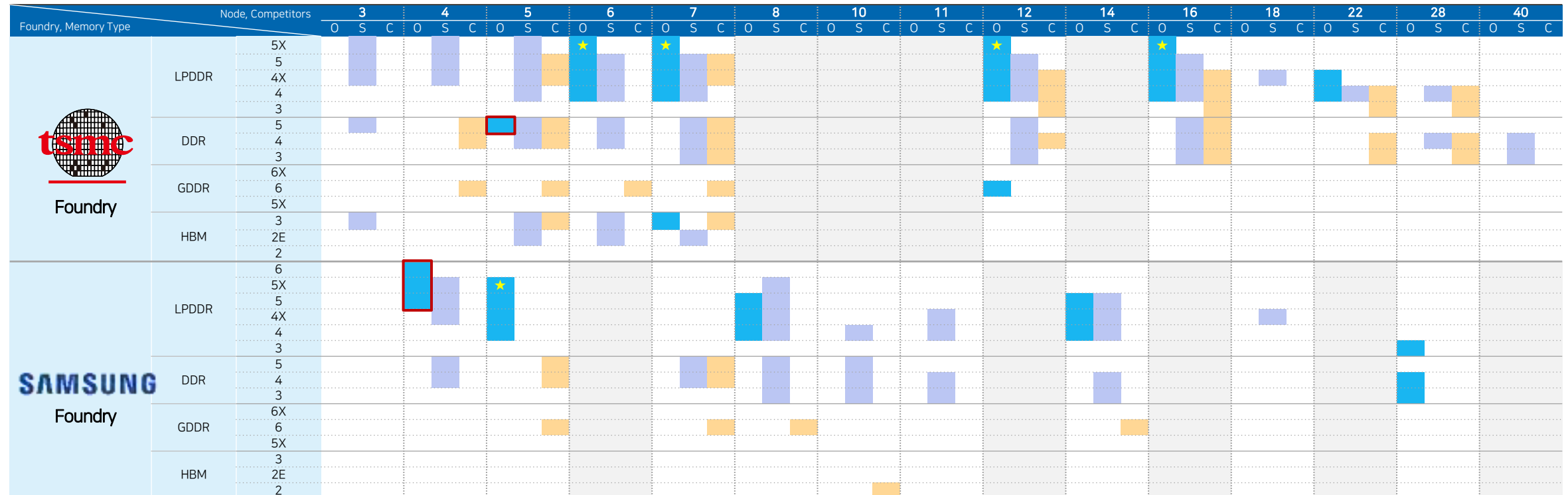
M/S expansion strategy

- ✓ Synopsys and Cadence are focusing on TSMC 5nm and below leading-edge processes
- ✓ OE is the only one provides LPDDR5X/5 PHY IP for various nodes
- ✓ OE is expecting customer pool through the development of PHY IP for SF 4nm & TSMC 5nm processes
- ✓ OE's PHY IP requires area less than 50% compared to competitors by providing through the test chips

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03 | Industry's Highest Technological Competitiveness ④

Maximize first-mover advantage of AI semiconductor integrated IP solutions

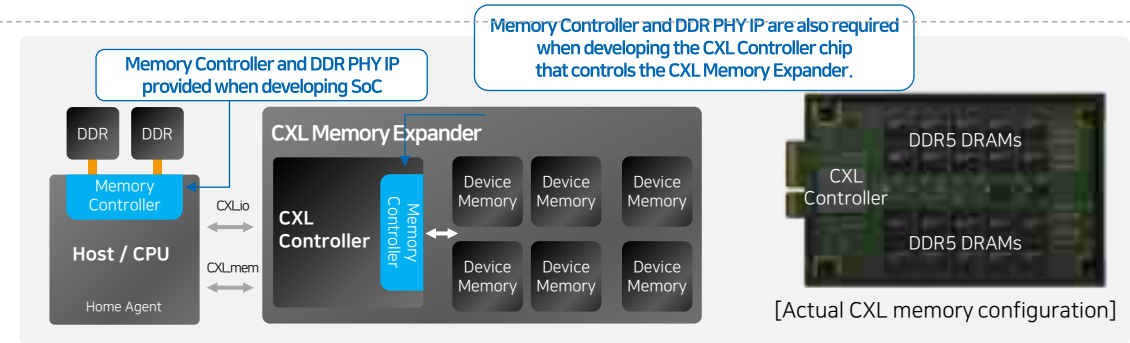| 예상 출시 일정	2021 1H	2021 2H	2022 1H	2022 2H	2023 1H	2023 2H	2024 1H	2024 2H	2025 1H	2025 2H
ENLIGHT™ Neural Processing Unit	NPU v1.0		NPU v2.0				NPU v3.0 (Autonomous Driving)		NPU4.0 (Autonomous Driving)	
	[Performance] 0.25~2 TOPS	[Target Product] Light-weight IoT application products (keyword recognition, security camera application)	[Performance] 2~16 TOPS	[Target Product] Medium or higher level of IoT application products (autonomous driving auxiliary application)	[Performance] 16~250 TOPS	[Target Product] High-performance application products for vehicles (Application of autonomous driving vehicles with Level 3 or higher)			[Performance] 250~1,000 TOPS	[Target Product] High-performance application products for vehicles (Multi-Die version application of autonomous driving vehicles with Level 4 or higher)
	Security Camera		Driver Support System		Fully Autonomous Driving					
OIC™ On-Chip Interconnect — Non-Cache Coherent NOC	OIC v. 1.X						OIC v.2.0			
OIC™ On-Chip Interconnect — Cache Coherent NOC									OIC-AI	
OMC™ Memory Controller	GDDR6	LP5X/5 /4X/4		HBM3	DDR5				LP6	
OPHY™ DDR PHY — SAMSUNG		LP4/4X/5 (14nm)			LP5X/5/4X (5nm)				LP6 (4nm)	
OPHY™ DDR PHY — tsmc			LP4/4X/5 GDDR6 (12nm)	LP4/4X/5 (22nm)	HBM3 LP4X/5/5X (6/7nm)		LP5X/5/4X (12/16nm)		DDR5 (5nm)	
OUC Controller Die to Die (Chiplet Controller)							UCIe v1.1 Controller (AXI streaming)		UCIe v1.1 Controller (Full spec.)	
OPHY™ PHY Die to Die (Chiplet) — SAMSUNG									OPHY-D2D (5/8nm)	
OPHY™ PHY Die to Die (Chiplet) — tsmc									OPHY-D2D (6nm)	

○ R&D started in 2023   ○ R&D to be launched from 2024

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03 | Industry's Highest Technological Competitiveness ⑤

Leading the next generation of high value-added semiconductor technology expected to grow rapidly
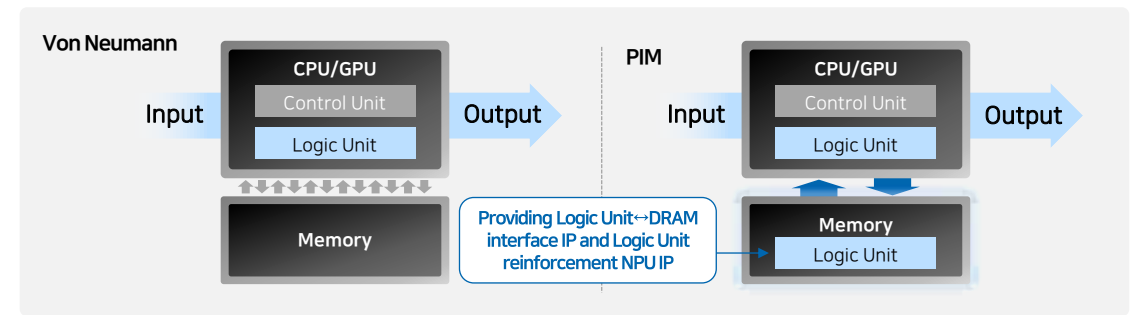
CXL (Compute eXpress Link)

- CXL interface can flexibly expand memory without limitations on memory standard capacity and performance dependent on existing Host/CPU
  → Effectively supports data intensive high-performance calculations such as AI chips
- supplies IP for the design of the CXL Controller chip, the core of the CXL Memory Expander.

Memory Controller and DDR PHY IP provided when developing SoC

Memory Controller and DDR PHY IP are also required when developing the CXL Controller chip that controls the CXL Memory Expander.

DDR | DDR
Memory Controller
Host / CPU
Home Agent
CXLio
CXL.mem

CXL Memory Expander
CXL Controller
Memory Controller
Device Memory | Device Memory | Device Memory
Device Memory | Device Memory | Device Memory

DDR5 DRAMs
CXL Controller
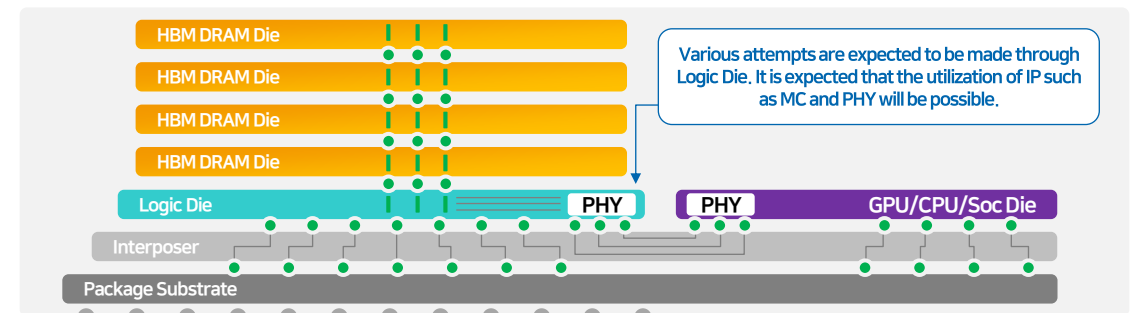DDR5 DRAMs
[Actual CXL memory configuration]

PIM (Process-in-Memory)

- PIM off-loads some of the computational functions handled by the Host/CPU (von Neumann structure) and processes them
  → Speed ↑ , Power ↓ by simultaneous calculation & storage
  ※ Samsung is using HBM and SK Hynix is using GDDR6 for developing PIM
- Supplies Memory System IP, which is responsible for the data interface between Logic Unit and DRAM in PIM semiconductors, and NPU IP required to improve the performance of Logic Unit.

Von Neumann
Input → CPU/GPU [Control Unit / Logic Unit] → Output
Memory

PIM
Input → CPU/GPU [Control Unit / Logic Unit] → Output
Memory [Logic Unit]

Providing Logic Unit↔DRAM interface IP and Logic Unit reinforcement NPU IP

HBM4

- Starting with HBM4, the Base Die is expected to be mounted as a Logic Die and utilize various functions
  → It is being attempted starting with HBM3E, but full-scale application is expected to start with HBM4.
- Currently, our main IPs such as Memory Controller and PHY are likely to be utilized.
  → Openedges already has HBM Memory Controller and PHY, and can customize those if requested by customers.

HBM DRAM Die
HBM DRAM Die
HBM DRAM Die
HBM DRAM Die
Logic Die | PHY
PHY | GPU/CPU/Soc Die
Interposer
Package Substrate

Various attempts are expected to be made through Logic Die. It is expected that the utilization of IP such as MC and PHY will be possible.

04 | Verified Global Track Records

Expanding global track record as value recognized as the essential solution in various industries

Number of licenses accumulated each year

Year	Licenses
2024. 2Q	59
2023	52
2022	40
2021	27
2020	17
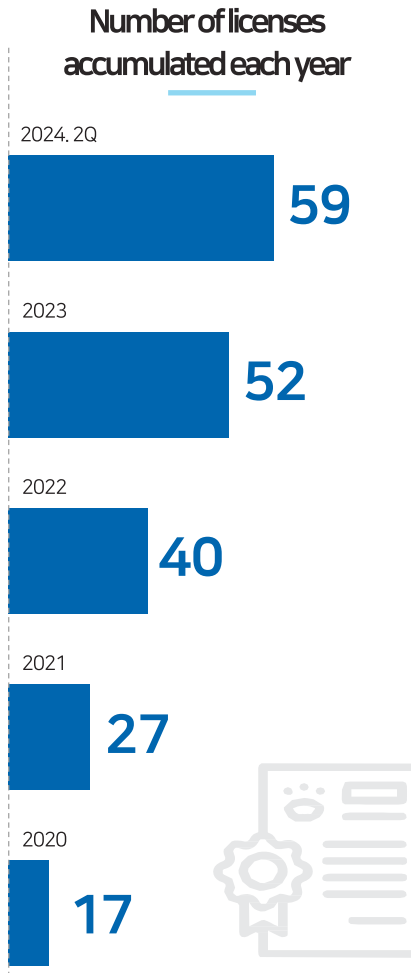
Intelligent security camera
VISIONEXT · nextchip · eyenix · DNP

Autonomous driving/ In-vehicle face recognition
AISIN · Telechips · nextchip · GAONCHIPS

Server/storage devices
SAMSUNG · SK hynix · 글로벌I社 · GLENFLY · asicland · novachips

IoT / Mobile
JLQ TECHNOLOGY · MONTAGE technology · SENSCOMM · GCT

AI
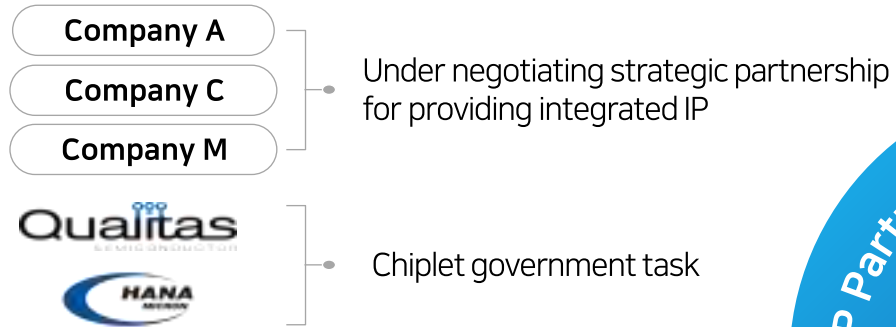Micron · VeriSilicon · SEMI FIVE · DEEPX

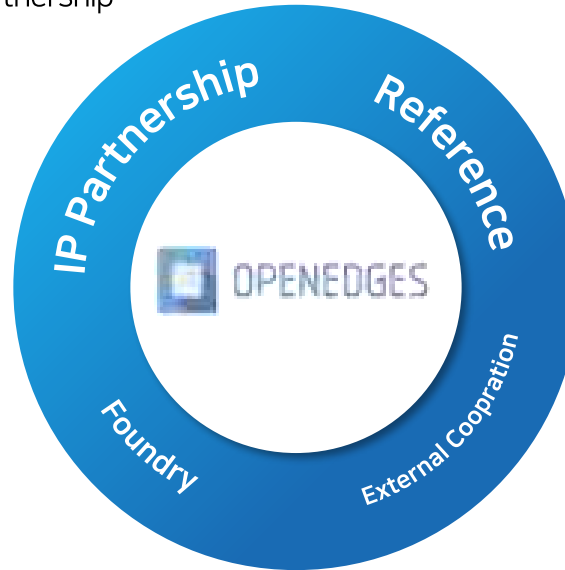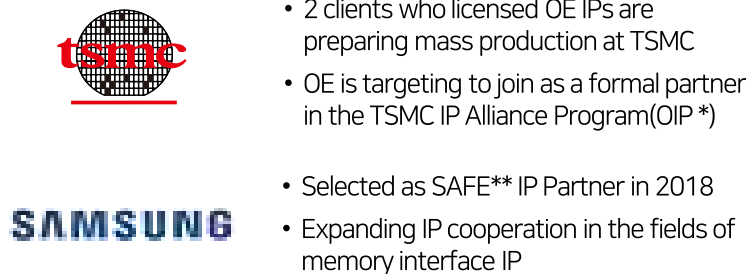**Others (drones, PC, etc.)**
LX Semicon · 티엘아이 · asicland

05 | Business Partnership with Global Enterprises

Securing stable IP demands + Proactive response to advanced technologies and market trends

Strengthening partnerships with IP companies

- Company A
- Company C
- Company M

Under negotiating strategic partnership for providing integrated IP

Qualitas
HANA

Chiplet government task

Strengthening partnerships with Foundries

tsmc

- 2 clients who licensed OE IPs are preparing mass production at TSMC
- OE is targeting to join as a formal partner in the TSMC IP Alliance Program(OIP *)

SAMSUNG

- Selected as SAFE** IP Partner in 2018
- Expanding IP cooperation in the fields of memory interface IP

IP Partnership / Reference / Foundry / External Coopration

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Securing references with top-tier customers

SAMSUNG   **SK hynix**   **Micron**

- Company I   **AISIN**   **alchip**

VeriSilicon   **MONTAGE Technology**   **JLQ TECHNOLOGY**

Strengthening external cooperation

HYUNDAI   Affiliates   **42dot**
Joint performance of Government autonomous driving project worth KRW 46 billion
bos

OPENEDGES   **SK**   Affiliates
IP License Contract
SAPEON
IP Government project
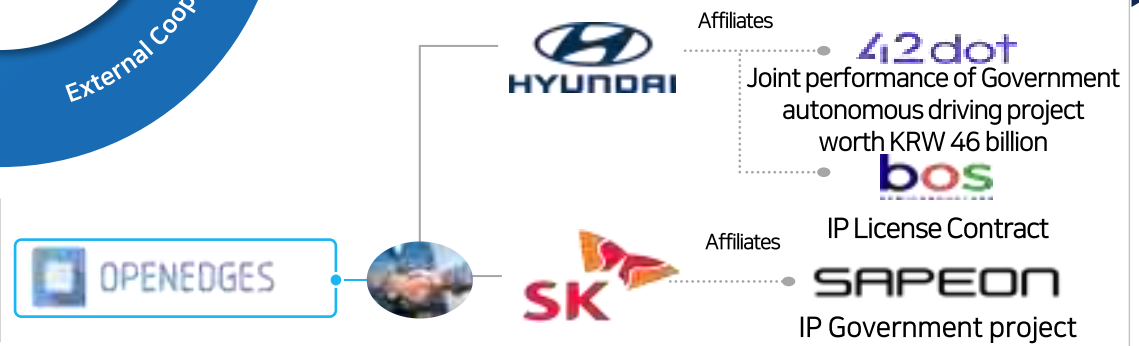
* OIP (Open Innovation Platform)
** SAFE (Samsung Advanced Foundry Ecosystem)

03

'24 2Q Business Performance

OPENEDGES

01 | Sales Revenue

'24 2Q sales recorded KRW 4 billion due to new contracts, etc., increase compared to the 1Q24(63.1%, QoQ), 2Q23(42.5%, YoY)
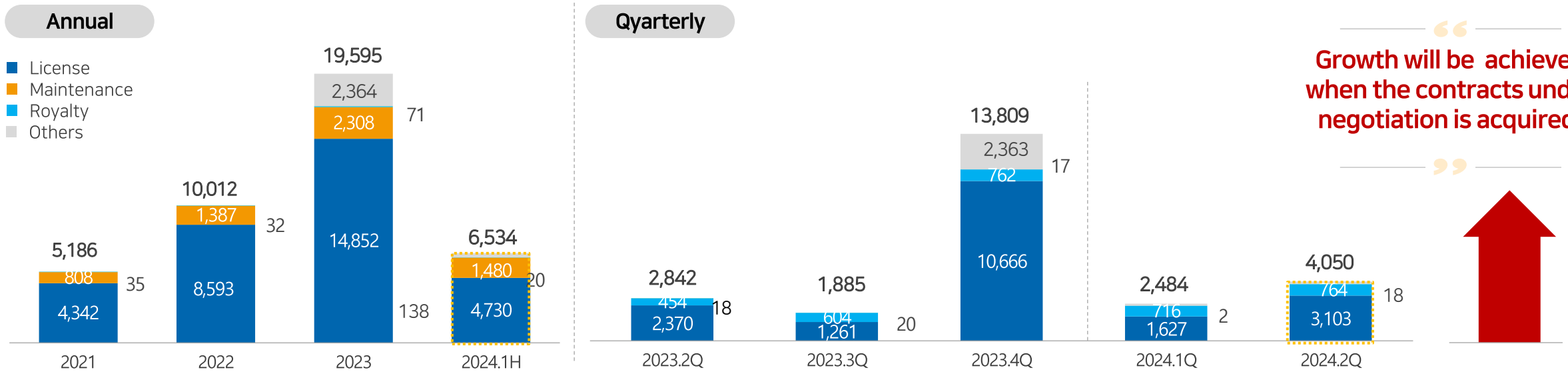
Sales status

(Unit: KRW 1 million)

Annual

- ■ License
- ■ Maintenance
- ■ Royalty
- ■ Others

	2021	2022	2023	2024.1H
Total	5,186	10,012	19,595	6,534
Others	35	32	71	20
			2,364	
Maintenance	808	1,387	2,308	1,480
License	4,342	8,593	14,852	4,730
				138

Qyarterly

	2023.2Q	2023.3Q	2023.4Q	2024.1Q	2024.2Q
Total	2,842	1,885	13,809	2,484	4,050
Others	18	20	17	2	18
			2,363		
Royalty	454	604	762	716	764
License	2,370	1,261	10,666	1,627	3,103

> **Growth will be achieved when the contracts under negotiation is acquired.**

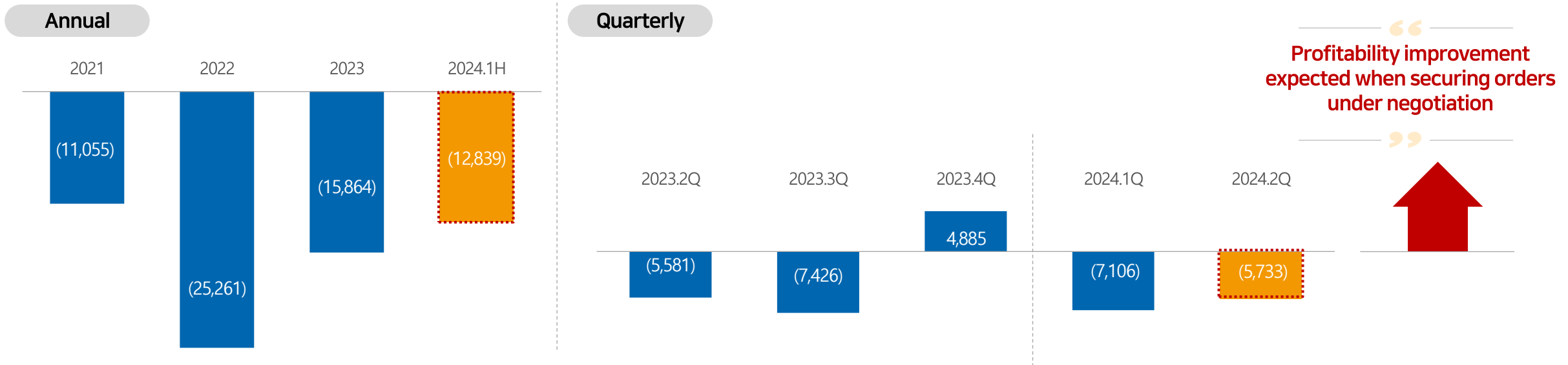### Sales Analysis

License	Revenue and ASP Increase due to new contracts and compared to 1Q24(QoQ) and 2Q23(YoY)
Maintenance	Sales are being generated from a total 32 projects
Royalty	Increased compared to 1Q24 and is expected to continue to rise steadily.
Others	Sales for operational and technical support services for Openedges Square

02 | Operating Profit(Loss)

Recorded a loss of 5.7 billion won, improved the deficit compared to1Q24
R&D expenses were managed at 8~9 billion won without much change

Operating Profit(Loss)

(Unit: KRW 1 million)

Annual

2021	2022	2023	2024.1H
(11,055)	(25,261)	(15,864)	(12,839)

Quarterly

Profitability improvement expected when securing orders under negotiation

2023.2Q	2023.3Q	2023.4Q	2024.1Q	2024.2Q
(5,581)	(7,426)	4,885	(7,106)	(5,733)

Operating Profit Analysis

- ✓ Sales increase reduces deficit compared to 1Q24, & deficit is expected to continue to decrease due to new contracts

- ✓ Most of the R&D expenses are for developing new IP, are being managed stably at around KRW 8 to 9 billion per quarter without burdening large one-off costs.

- ✓ Currently, discussions are underway to acquire multiple licenses, and sales growth and profitability improvement are expected to continue.

03 | Contract Status

Contract value Increase QoQ due to the high-performance IP contracts.
It will continue to grow due to closing of contracts under negotiation in 2H24.

Contract Status

(Unit: USD 1 million)

☐ **'24.2Q: 4 new license contracts, worth $5.3M**

- The average price per contract is $1.3M,
- Winning a high-performance/high-price IP contracts

☐ **'24.1H: 7 cumulative license contracts, worth $7.4M**

- Cumulative contract value increase 68% compared to 1H23($4.4M)
- ASP per contract was $1.1M, increased from $0.7M in 1H23.

Contract status

(Unit: case/$M)	'24.2Q (3M)	'24.1H (6M)	'23.1H (6M)	FY2023	FY2022
Numbers	4	7	6	12	13
Sum of Contract value	$5.3M	$7.4M	$4.4M	$15.5M	$7.5M
Average price per Contract	$1.3M	$1.1M	$0.7M	$1.3M	$0.6M

Performance Analysis and outlook

'24 2Q Results

☐ **Signing high-performance/high-price IP contract**

- Winning high-performance SoC projects considering Samsung 5nm, etc.

☐ **Delay in completion of customization design project**

- Negotiation on customized IPs that support the latest DRAMs such as HBM3 and DDR5 took longer than expected

Outlook for the second half of 2024

☐ **Expect high growth in normal license sales and improve profitability**

- Securing large orders from Tier-1 customers in 2H of 2024
- Improving sales and profitability with high-performance IP-centered IP order contracts
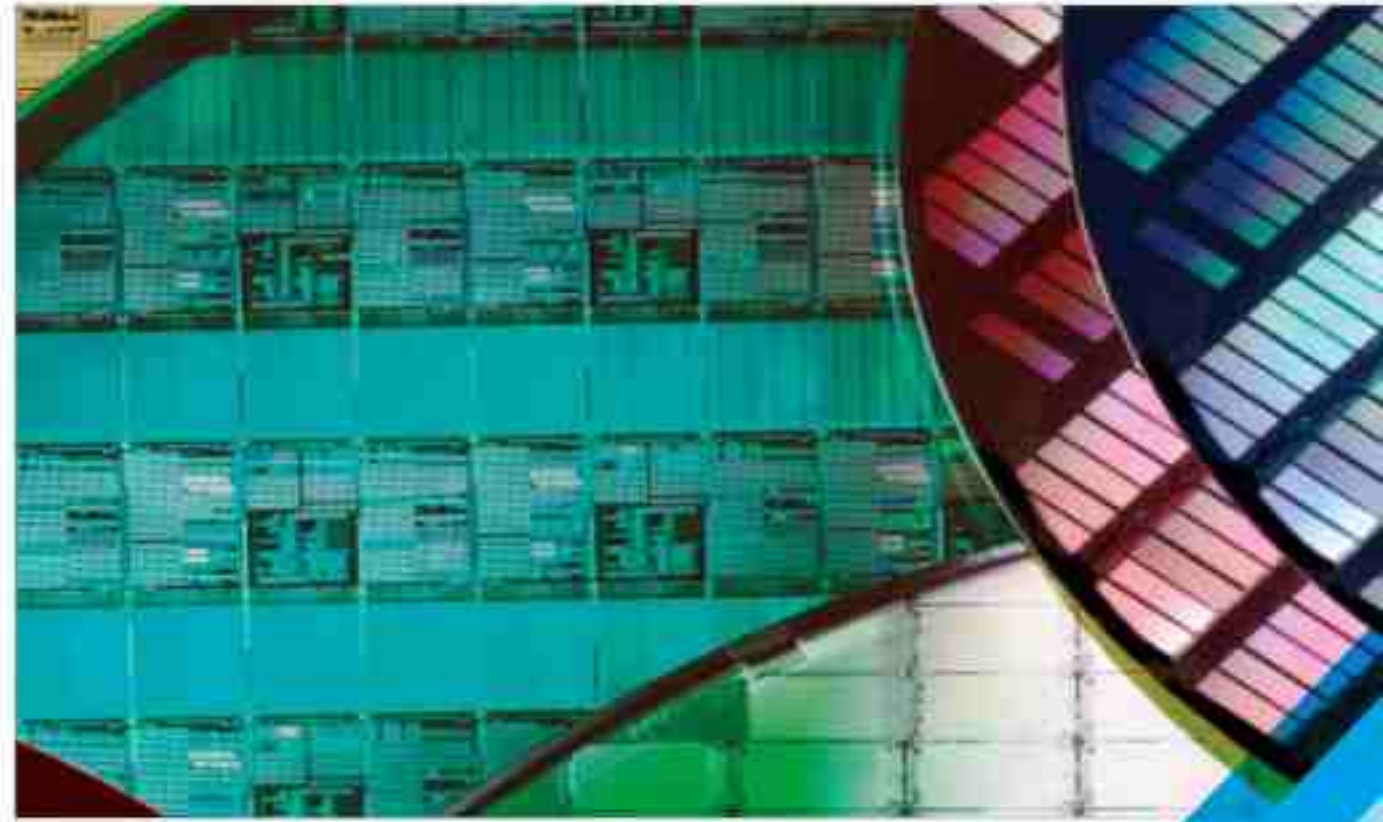
☐ **Expand due to demand for next-generation and customization**

- In addition to CXL, expanding collaboration to reduce the performance gap between AI semiconductors and DRAM, such as PIM and Chiplet
- In addition to normal licenses, we plan to respond quickly to customization IP licenses with global top-tier companies

04

Growth Strategy

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01 │ Growth Plan

**Expanding Portfolio with
AI Semiconductor IP Solution**

Multi Die/Chip ┈┈┈┈┈┈┈┈┈┈

On-die ┈┈┈┈┈┈┈┈┈┈
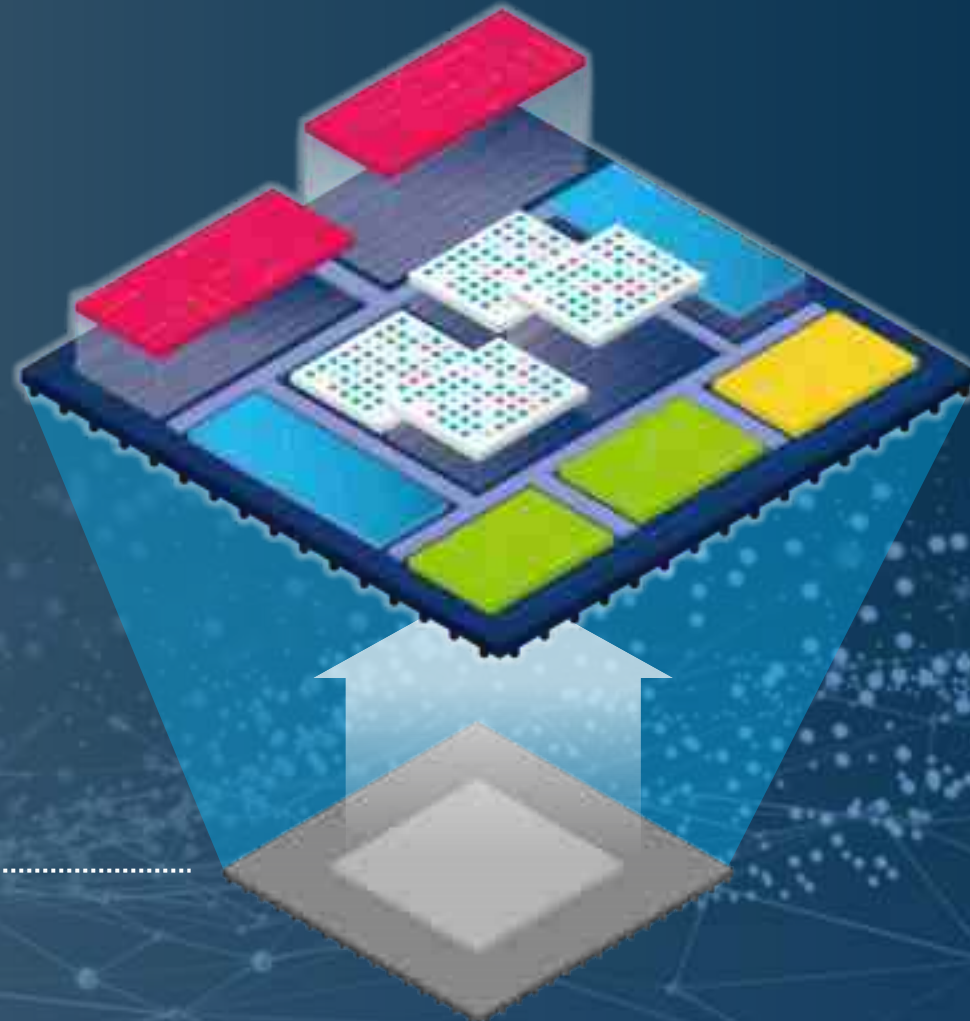
02 | Strengthen existing IP competitiveness

Improving performance and Expansion of existing IP products

OPENEDGES

DDR DRAM

AI semiconductor

+ LLM and SLM support & expansion to high performance

* LLM : Large Language Model
SLM : Small Language Model

MEMORY CONTROLLER

PHY
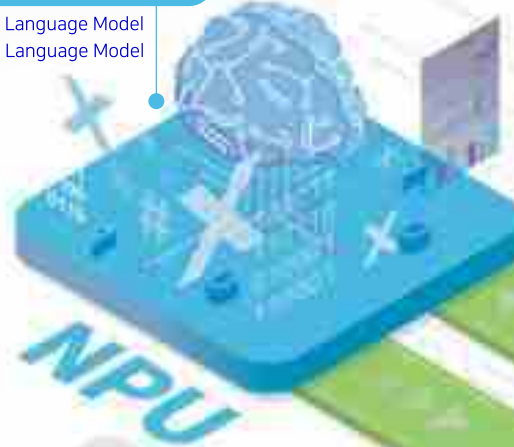
+ Porting House Operation→ Expanding Foundry Process Coverage

* PHY Porting House: Responsible for simple repetitive tasks (layout, etc.), reviewing establishment of a subsidiary in Vietnam or Eastern Europe

NPU

ON CHIP INTERCONNECT

+ Cache Coherence Network-on-Chip IP in development

* IP responsible for maintaining data consistency in the cache memory within the SoC, a technology required when designing high-performance AI semiconductors based on multi-core

+ IP Verification Subsidiary Operation→ IP Release Capacity Expansion, Cost Efficiency Improvement

* Considering establishment of a subsidiary in Vietnam or Eastern Europe

03 | Expand detailed IP Portfolio

Expanding to a Total IP Solution that connects Multi-Die and Multi-Chip

GPU

UCIe

Next-generation interconnect technology for high-speed data communication between chips

Memory Module (CXL etc.)

PCIe

A high-speed interface standard for data transfer between various devices within a computer system

Chiplet PKG

NPU Accelerator

Main AP

DDR DRAM

Memory Chiplet

A high-speed interface standard for data transfer between various components on mobile devices

MIPI

Storage

USB

A universal serial bus for data transfer and power supply between computers and peripheral devices

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04 | Why Expanded IP Portfolio? ① Rapid growth of the Wired Interface IP market

Wired Interface IP sector is growing the fastest due to increasing data demand for AI computing

Market Size by Semiconductor IP Market Segment

(Unit: $M)

2019	2020	2021	2022	2023
3,944	4,567	5,522	6,665	7,050
873	1,038	1,307	1,660	1,756

Wired Interface IP
CAGR (2019~2023)
19%

Market Share by Semiconductor IP Market Segment

(Unit: %)

- 2019: 22%
- 2021: 24%
- 2023: 25% (3%)

Wired Interface IP
Change(%)
+3%p

■ CPU IP ■ GPU, ISP IP ■ Wired Interface IP ■ System IP ■ Other IP
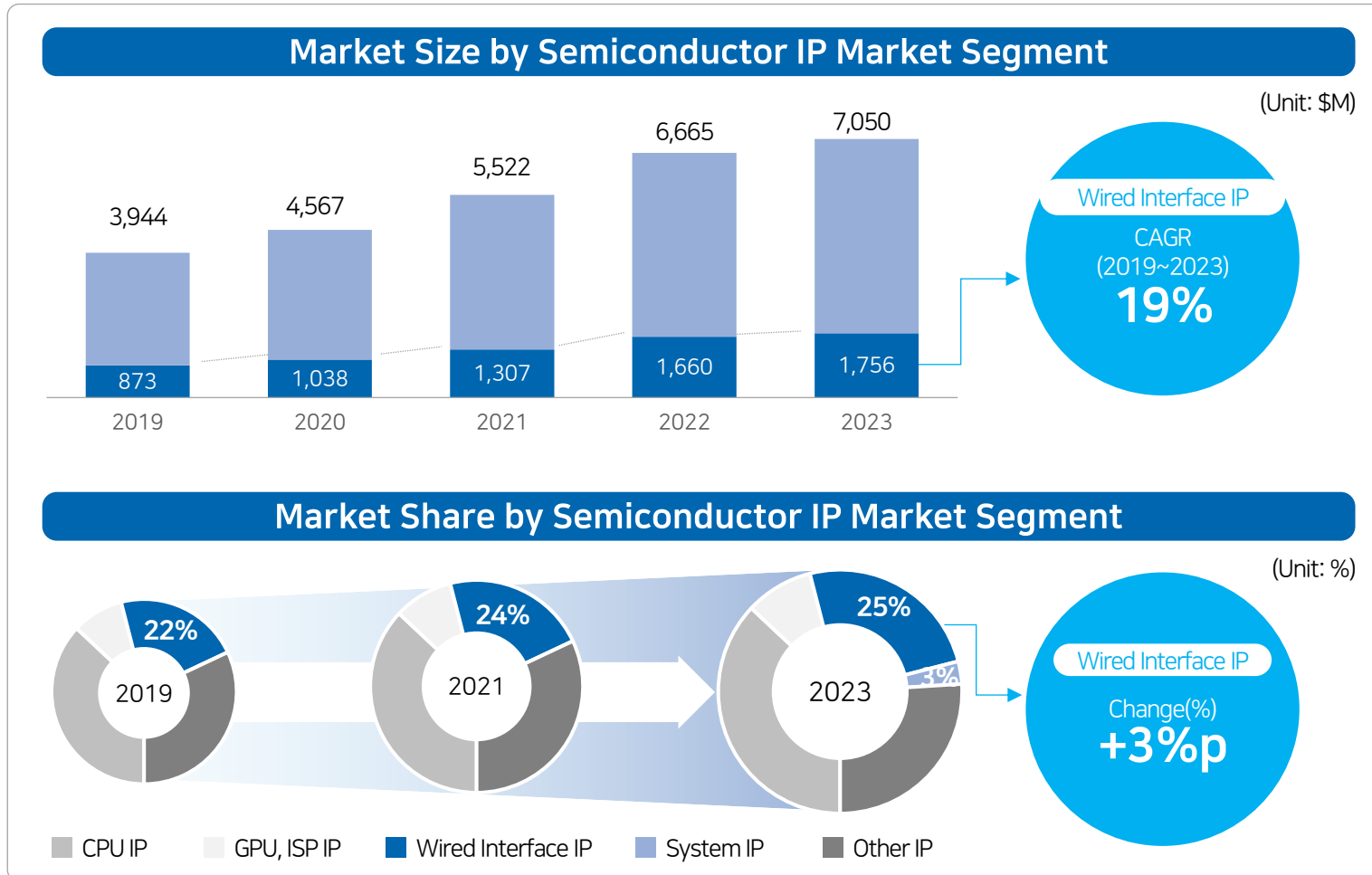
Wired Interface IP Growth Factors

Explosive Increase in Data Bandwidth Demand for AI
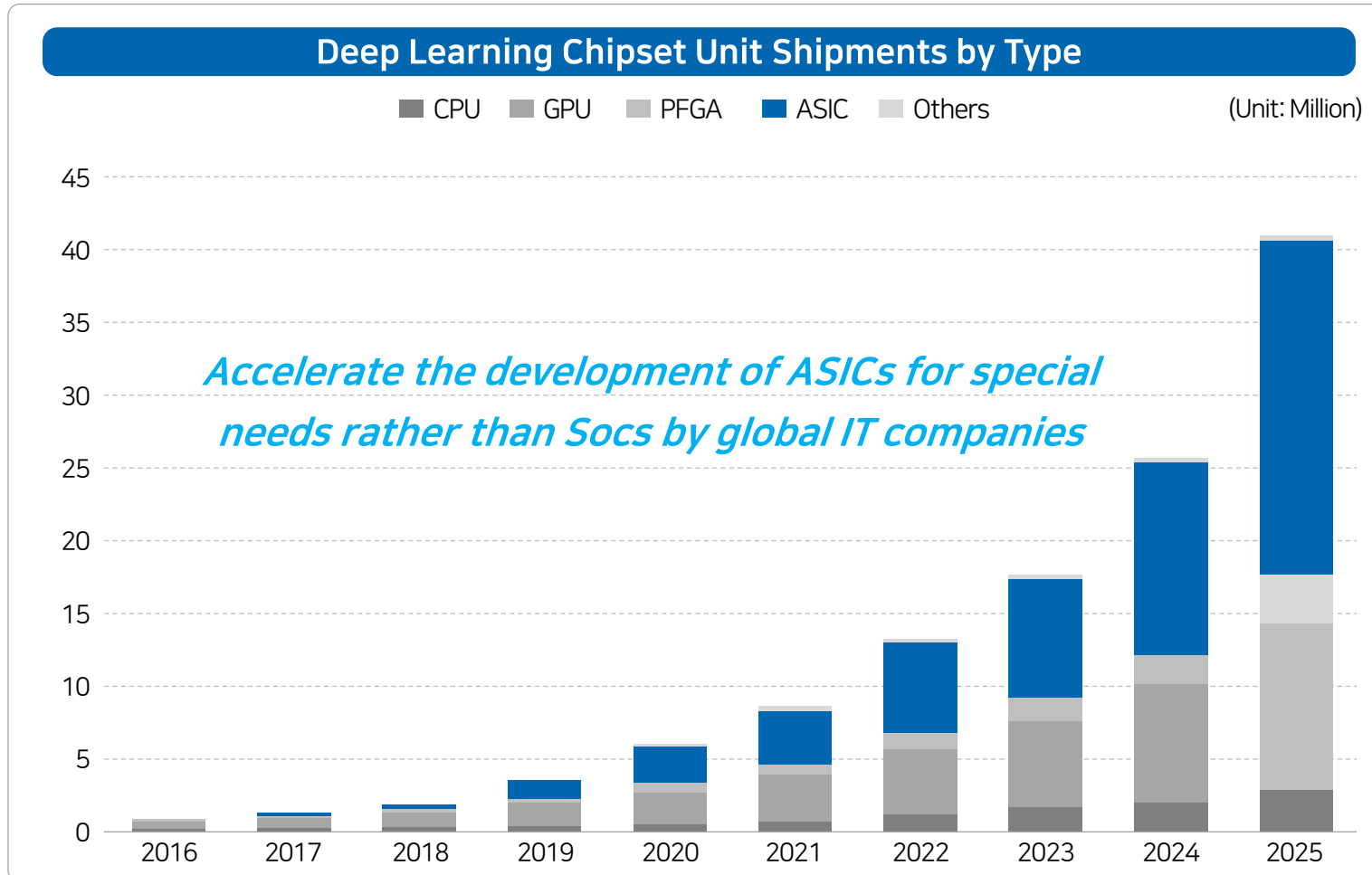
New memory standards → IP prices rise sharply

Oligopoly market system (Only 3players including Openedges)

※ Resources: IPnest (As of May, '24)

04 | Why Expanded IP Portfolio? ② Responding to demand for customized AI semiconductor chips (ASIC)

AI semiconductor market paradigm shift from SoC to ASIC
→ Increased need for cooperation with semiconductor IP companies

Deep Learning Chipset Unit Shipments by Type

■ CPU   ■ GPU   ■ PFGA   ■ ASIC   ■ Others

(Unit: Million)

Accelerate the development of ASICs for special needs rather than Socs by global IT companies
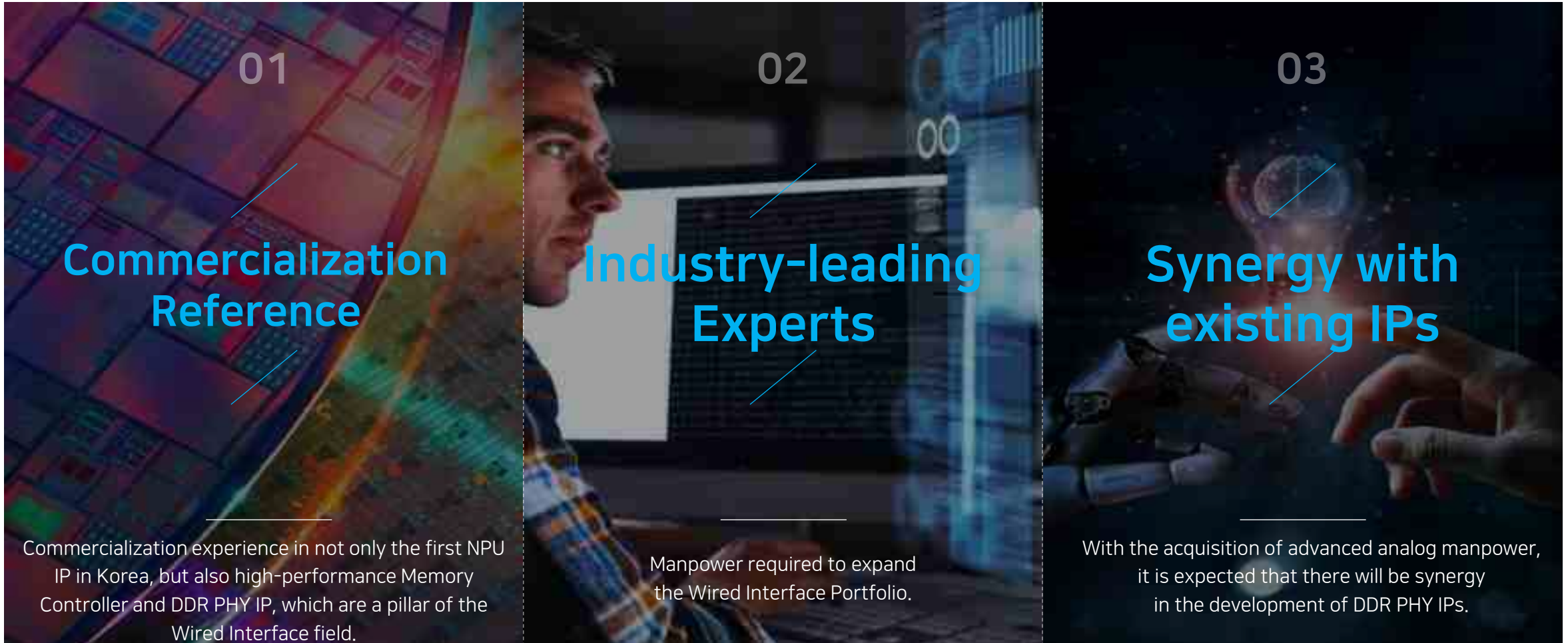

Resources: Tractica

Factors in demand for ASIC

Need for complex neural network response capable of complex natural language processing such as LLM/SLM

Design optimization from a whole chip perspective is needed to support data intensive computing

05 | How to Succeed?

Openedges has already secured industry-leading human resources and commercialization reference

01

Commercialization Reference

Commercialization experience in not only the first NPU IP in Korea, but also high-performance Memory Controller and DDR PHY IP, which are a pillar of the Wired Interface field.

02

Industry-leading Experts

Manpower required to expand the Wired Interface Portfolio.

03

Synergy with existing IPs

With the acquisition of advanced analog manpower, it is expected that there will be synergy in the development of DDR PHY IPs.

06 | Comparing Competitor IP Portfolios

By commercializing each IP in the Wired Interface IP field sequentially, Openedges will build up the Total AI Platform IP Solution optimized with ENLIGHT NPU by 2030.
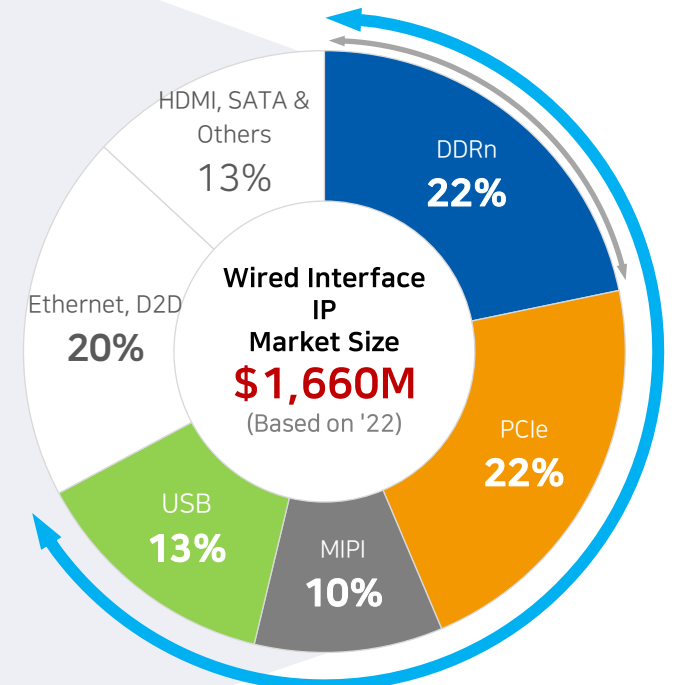
Global Top 5 IP Companies vs. Openedges

IPs			Openedges	arm	Synopsys	Cadence	Alphawave Semi	Imagination Technologies
Processor IP	CPU (Central Processing Unit)		-	●	●	-	-	●
	GPU, ISP (Image Signal Processor)		-	●	* RISC-V	-	-	●
	DSP (Digital Signal Processor)		-	-	●	●	-	-
	NPU (Neural Processing Unit)		●	○	○	○	-	●
Physical IP	Wired Interface IP	DDR Cont'r/PHY	●	-	●	●	-	-
		HBM Cont'r/PHY	●	-	●	●	●	-
		UCIe Cont'r/PHY	★	-	●	●	●	-
		PCIe Cont'r/PHY	★	-	●	●	●	-
		CXL Cont'r/PHY	★	-	●	●	●	-
		Ethernet	-	-	●	●	●	-
		USB	★	-	●	●	-	-
		SATA(Serial ATA)	-	-	●	●	-	-
		HDMI	-	-	●	●	-	-
		Display Port	-	-	●	●	-	-
		MIPI	★	-	●	●	-	-
	Memory Compilers (Others)		-	-	●	-	-	-
	Standard Cell & I/O		-	●	●	-	-	-
	Memory Compilers (SRAM)		-	●	●	-	-	-
	Analog & Mixed Signal		-	-	●	●	-	-
	Wireless Interface IP		-	-	●	●	-	-
Other Digital IP	Miscellaneous IP		-	-	●	●	-	-
	System IP (CC NoC, NCC NoC 등)		●	●	○	○	-	-
	Security IP		-	●	●	-	-	-

* ○: We judge the company to be a non-major competitor with little history of competition in the market (focused on low-end)

★: Candidates for Openedges ★: FY 2025 / ★: FY 2026 / ★: FY2027~

Expanding market coverage

22% ❯ 67%

Wired Interface IP Market Size $1,660M (Based on '22)

- DDRn **22%**
- PCIe **22%**
- MIPI **10%**
- USB **13%**
- Ethernet, D2D **20%**
- HDMI, SATA & Others **13%**

※ The D2D (UCIe) market is expected to grow rapidly in the future due to the increase in demand for chiplet development, although the market size in 2022 is small and difficult to distinguish from Ethernet.

[Appendix] Financial Statements(Consolidated)

Statement of Financial Position

(Unit: KRW 1 million)

	2Q24	2023	2022	2021
Current Assets	22,449	29,843	44,304	29,020
Non-current Assets	11,216	14,849	9,552	7,077
Total Assets	**33,664**	**44,692**	**53,855**	**36,097**
Current Liabilities	18,662	19,750	18,318	9,171
Non-current Liabilities	4,972	4,371	3,288	6,374
Total Liabilities	**23,634**	**24,121**	**21,606**	**15,545**
Capital	2,184	2,146	2,116	1,653
Capital Surplus	100,573	98,259	96,376	58,927
Other Capital	3,552	3,577	2,026	3,007
Retained earnings	△96,279	△83,412	△68,269	△43,035
Total Equity	**10,031**	**20,571**	**32,249**	**20,553**

Income Statements

(Unit: KRW 1 million)

	2Q24	1Q24	Change	Change(%)
Sales Revenue	4,050	2,484	1,566	63%
Operating Expenses	9,784	9,589	195	2%
R&D Cost	7,816	7,543	273	4%
Selling General & Admin. Expense	1,968	2,046	△78	△4%
Operating Profit	△5,733	△7,106	1,373	*N/A*
Financial Income	285	380	△95	△25%
Financial Expenses	347	416	△69	△17%
Other Income	35	37	△2	△5%
Other Costs	1	–	1	*N/A*
Profit before Income Tax Expense	△5,762	△7,106	1,344	*N/A*
Income Tax Expense	–	–	–	*N/A*
Net Income	△5,762	△7,106	1,344	*N/A*

Financial Summary

(Unit: KRW 1 Million)

Consolidated	2019	2020	2021	1Q22	2Q22	3Q22	4Q22	2022	1Q23	2Q23	3Q23	4Q23	2023	1Q24	2Q24
Revenue	1,238	1,089	5,186	3,033	3,975	1,577	1,426	10,012	1,059	2,842	1,885	13,809	19,595	2,484	4,050
License fee	990	660	4,342	2,798	3,619	1,175	1,001	8,593	555	2,370	1,261	10,666	14,852	1,627	3,103
Maintenance	249	423	808	230	350	392	415	1,387	487	454	604	762	2,308	716	764
Royalty	-	6	35	5	7	10	10	32	17	18	20	17	71	2	18
Others	-	-	-	-	-	-	-	-	-	-	-	2,363	2,363	138	166

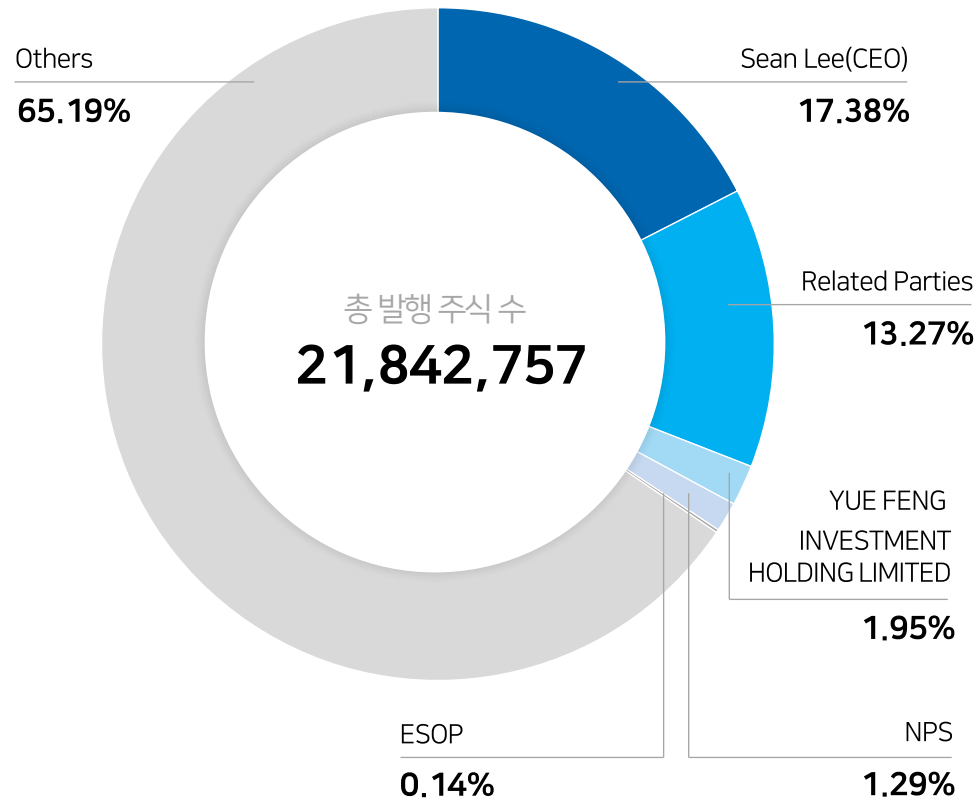| Consolidated	2019	2020	2021	1Q22	2Q22	3Q22	4Q22	2022	1Q23	2Q23	3Q23	4Q23	2023	1Q24	2Q24
Cost and Expense	4,422	8,896	16,241	5,792	7,293	7,844	14,344	35,273	8,801	8,422	9,311	8,924	35,458	9,589	9,784
R&D Cost	2,347	6,623	10,654	3,937	5,361	6,063	12,349	27,710	7,052	6,546	7,146	6,439	27,184	7,543	7,816
Selling General & Admin Expense	2,075	2,273	5,587	1,855	1,932	1,782	1,995	7,563	1,749	1,876	2,165	2,485	8,275	2,046	1,968
Operating Income	△3,183	△7,807	△11,055	△2,759	△3,317	△6,267	△12,918	△25,261	△7,742	△5,581	△7,426	4,885	△15,864	△7,106	△5,733
Net Profit before Corporate Tax Costs	△8,487	△18,729	△14,524	△2,906	△3,398	△6,181	△12,362	△24,846	△7,634	△5,559	△7,317	6,000	△14,510	△7,106	△5,762
Net Income	△8,487	△18,729	△14,608	△2,906	△3,398	△6,178	△12,745	△25,227	△7,631	△5,557	△7,310	5,642	△14,856	△7,106	△5,762

※ Numbers are based on consolidated financial statements.

[Appendix] Shareholders

Sean Lee(CEO, 17.38%) & related parties own more than 30%(30.65%)

* Co-founders, Executives etc.

Shareholder Status ('24.6.30.)

총 발행 주식 수
21,842,757

Others **65.19%**
Sean Lee(CEO) **17.38%**
Related Parties **13.27%**
YUE FENG INVESTMENT HOLDING LIMITED **1.95%**
ESOP **0.14%**
NPS **1.29%**

Name	Type	# of shares	%
Sean Lee(CEO)	Common	3,796,314	17.38%
Related Parties	Common	2,899,543	13.27%
YUE FENG INVESTMENT HOLDING LIMITED	Common	425,000	1.95%
NPS (National Pension Service)	Common	281,706	1.29%
ESOP	Common	30,980	0.14%
Others	Common	14,239,308	65.19%
Total		**21,842,757**	**100.00%**

※ Date: '24.6.30.

※ Reference: '24.7.22, Stonebridge and Atinum each acquired 1,474,853 shares of convertible preferred stock by issuing new stocks allocation to the third-parties.